Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (currently amended) A memory device, comprising:

a first conductive layer, wherein a portion of the first conductive layer acts as a source region for the memory device;

a conductive structure having a ~~substantially~~ cylindrical shape formed on the first conductive layer, the conductive structure having a first end and a second end opposite the first end, wherein the first end is disposed adjacent the portion of the first conductive layer that acts as the source region for the memory device and wherein the second end acts as a drain region for the memory device;

a plurality of dielectric layers formed around at least a portion of the conductive structure, wherein at least one of the dielectric layers acts as a floating gate electrode for the memory device; and

a control gate formed over the plurality of dielectric layers, and

wherein a top portion of the second end of the conductive structure does not contact any of the plurality of dielectric layers.

2. (canceled)

3. (previously presented) The memory device of claim 1, wherein the conductive structure has a thickness ranging from about 100 Å to about 1000 Å and a width ranging from

about 100 Å to about 1000 Å.

4. (previously presented) The memory device of claim 1, further comprising:

an insulating layer formed on the first conductive layer, the insulating layer contacting the first end of the conductive structure.

5. (original) The memory device of claim 1, wherein the plurality of dielectric layers comprises:

a first oxide layer formed around the conductive structure,

a nitride layer formed around the first oxide layer, and

a second oxide layer formed around the nitride layer, wherein the nitride layer acts as the floating gate electrode.

6. (original) The memory device of claim 5, wherein the first oxide layer has a thickness ranging from about 100 Å to about 500 Å, the nitride layer has a thickness ranging from about 100 Å to about 500 Å, and the second oxide layer has a thickness ranging from about 100 Å to about 500 Å.

7. (original) The memory device of claim 1, wherein the plurality of dielectric layers has a combined thickness ranging from about 300 Å to about 1500 Å and functions as a charge storage structure.

8. (original) The memory device of claim 1, wherein the control gate comprises polysilicon and has a thickness ranging about 100 Å to about 1000 Å.

9. (original) The memory device of claim 1, further comprising:

a substrate; and

a buried oxide layer formed on the substrate, wherein the first conductive layer is formed on the buried oxide layer.

10. (currently amended) A memory device, comprising:

a substrate;

a first insulating layer formed on the substrate;

a conductive structure having a ~~substantially~~ cylindrical shape formed over the first insulating layer, the conductive structure functioning as a channel region for the memory device;

a plurality of dielectric layers formed around a lower and a middle portion of the conductive structure and not around an upper most portion of the conductive structure, at least one of the dielectric layers functioning as a charge storage electrode for the memory device; and

a control gate formed over the plurality of dielectric layers, and

wherein a top portion of the conductive structure does not contact any of the plurality of dielectric layers.

11. (previously presented) The memory device of claim 10, further comprising:

a conductive layer formed between the first insulating layer and the conductive structure, wherein a portion of the conductive layer adjacent the conductive structure acts as a source region for the memory device.

12. (original) The memory device of claim 10, wherein the plurality of dielectric layers comprises:

a first oxide layer formed around at least a portion of the conductive structure,

a nitride layer formed around the first oxide layer, and

a second oxide layer formed around the nitride layer, wherein the nitride layer acts as the charge storage electrode.

13. (previously presented) The memory device of claim 10, wherein a first end of the conductive structure acts as a drain region for the memory device.

14. (original) The memory device of claim 10, wherein the plurality of dielectric layers has a combined thickness ranging from about 300 Å to about 1500 Å.

15. (currently amended) The memory device of claim ~~10~~ 11, further comprising:

a second insulating layer formed on the ~~first~~ conductive layer, the second insulating layer contacting a lower most portion of the conductive structure.

16. (currently amended) A non-volatile memory array, comprising:

a first conductive layer formed on a substrate, wherein portions of the first conductive layer act as source regions for memory cells in the memory array;

a plurality of structures formed on the first conductive layer, wherein each of the plurality of structures has a ~~substantially~~ cylindrical shape and functions as a channel region for one of the memory cells;

a plurality of dielectric layers formed around portions of each of the plurality of structures, wherein at least one of the plurality of dielectric layers functions as a charge storage electrode for one of the memory cells; and

at least one conductive layer formed over the plurality of dielectric layers for each of the memory cells, and

wherein a top portion of each of the plurality of structures does not contact any of the plurality of dielectric layers.

17. (original) The non-volatile memory array of claim 16, wherein the plurality of dielectric layers comprises:

a first oxide layer,

a nitride layer formed around the first oxide layer, and

a second oxide layer formed around the nitride layer, wherein the nitride layer functions as the charge storage electrode.

18. (original) The non-volatile memory array of claim 16, further comprising:

a plurality of bitlines, wherein each of the plurality of bitlines contacts a

number of the plurality of structures.

19. (original) The non-volatile memory array of claim 18, wherein the at least one conductive layer comprises a plurality of conductive layers, wherein each of the conductive layers contacts a top one of the plurality of dielectric layers associated with a group of memory cells and functions as a word line for the non-volatile memory array.

20. (previously presented) The non-volatile memory array of claim 16, wherein each of the plurality of structures functions as a drain region for one of the memory cells.

21. (previously presented) The non-volatile memory array of claim 16, further comprising:

an insulating layer formed on the first conductive layer, the insulating layer contacting a lower portion of the plurality of structures.